Scope International Journal of Science, Humanities, Management and Technology. ISSN : 2455-068X
Vol.2 Issue 2 (2016) 102-105. Submitted 28/03/2016. Published 05/04/2016

IMPLEMENTATION OF CASCADED H BRIDGE INVERTER FOR SINGLE PHASE AC MOTOR DRIVE

[1]S.P.Ganesh, [2]P.Venkatesh, [3]C.Yuvaraj, [4]M.Sudhakaran,
[1,2,]Dept of EEE, GTEC Engg. College, Vellore,
[3]Asst. Prof, Dept of EEE, GTEC Engg. College, Vellore,
[4]Associate Prof, Dept of EEE, GTEC Engg. College, Vellore.

Abstract:
This paper presents the implementation of Single Phase 7 level Multilevel DC link (MLDCL) Inverter with Half Bridge Cell topology. For N level inverter, (N-1)/2 half bridge cells are required with the same number of voltage sources. In this inverter topology, 3 Half Bridge Cells are used along with 3 voltage sources, each have 100V DC. These half bridges are connected in series to form a Multilevel DC Link (MLDCL). Power IGBTs are used as switching device. Each half bridge cell uses two IGBTs whereas H-Bridge requires four IGBTs. In this inverter topology, eight Power IGBTs along with gate drive circuit. Inverter topology, under study reduced power switches. The performance of inverter checked on single phase induction motor. THD of proposed topology is reduced and analyzed by FFT window. The results are observed by MATLAB/SIMULINK software.

Keywords- Cascaded Multilevel Inverter, Multilevel DC Link, Cascaded Half Bridge Cells, H Bridge, Total Harmonic distortion (THD).

1. INTRODUCTION

In present era, there is huge demand of medium and high power in industries. They require improved speed control methods power quality to run motors in industries. When an in inverter fed an ac motor drive system, harmonics cause losses and pulsating torque in the motor. From the energy saving viewpoint, it is necessary to develop a high efficiency motor drive system. Multilevel inverter is used. it has many improved features then the two level inverter. The Multilevel inverters are basically three types, which are as 1) Diode clamped MLI, 2) Flying Capacitor MLI and 3) Cascaded H-bridge MLI [1-2]. Advantages of the multilevel inverters (MLIs) include: 1) the multilevel structures can ensure even voltage sharing, both statically and dynamically, among the active switches while it is difficult for a two-level inverter with a series connection of switches to do so; 2) substantial reduction in size and volume is possible due to the elimination of the bulky coupling transformers or inductors; and 3) multilevel inverters can offer better voltage waveforms with less harmonic contents and thus, can significantly reduce the size and weight of passive filter components. This paper presents a new class of multilevel inverters based on an MLDCL and a bridge inverter[5]. In this paper we uses Cascaded H-bridge along with the half bridge topology to get the single phase seven level output voltage. The main bridge is cascaded H-bridge MLI which have four power switches and there are two half bridge cell which have only four power switches along with three same voltage sources. The Cascaded H-bridge MLI is shown in fig 1, for 7 level output voltage needed twelve power switches [3]. An induction motor is used as main load to perform the inverter output with LC filter.

2. MODIFIED CONVERTER TOPOLOGY

Modified inverter topology, which consists of a multilevel DC source and a single-phase full-bridge inverter [4]. The DC source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches. The two switches S(n-1)1 and S(n-1)2 operate in a

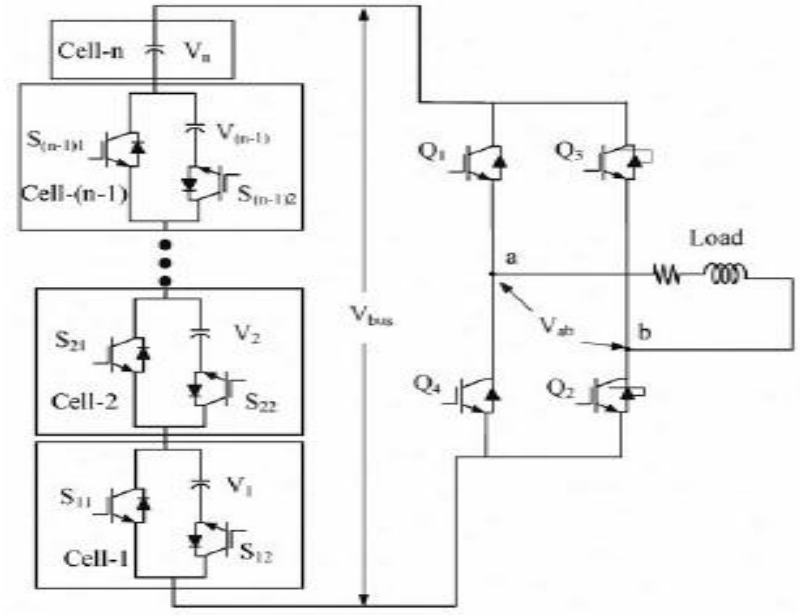

Fig.1. Structure of the proposed cascaded dc link MLI.

toggle fashion. The cell source is bypassed with S(n-1)1 ON and S(n-1)2 OFF, or adds to the DC-link voltage by reversing the switches [5]. In modified topology the main single phase H-bridge system composes of four switches Q1, Q2, Q3 and Q4. The H-bridge inverter has two functions, it has to synthesis the inversion voltage of the dc link voltage plus generating the zero state voltage (OV) at the output voltage (Vab) by connecting the upper two switches (Ql, Q3) or the lower switches . Working of this inverter is nothing but how we make IGBTs ON and OFF. We have generated a switching sequence to obtain staircase output which resembles nearly equal to sine wave. For different switching angles the power circuit behaves differently producing different waveforms. In this topology, we have generated 7 voltage levels as 0, 100V, 200V, and 300V.

3. CONTROL SCHEME

Here we have used the pulse generator to generate the different switching waves to control the IGBT power switches. The smooth sine wave is produced by selecting the proper value of firing angles in pulse generator. Here is the different switching pulse is generated by pulse generator is shown in fig 2. In this topology there are total 8 IGBT is used to generate the desired 7 level output voltage across the load and the gate driver circuit needed is also eight required here. The gate driver circuit is pulse generator, which produces different pulses as per desired requirement to generate the 7 level output. In this paper we uses an induction motor to analyze the motor main winding current, rotor speed and Electromagnetic torque, also observing the output voltage and total harmonic distortion(THD). The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated. In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages. In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H-bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is

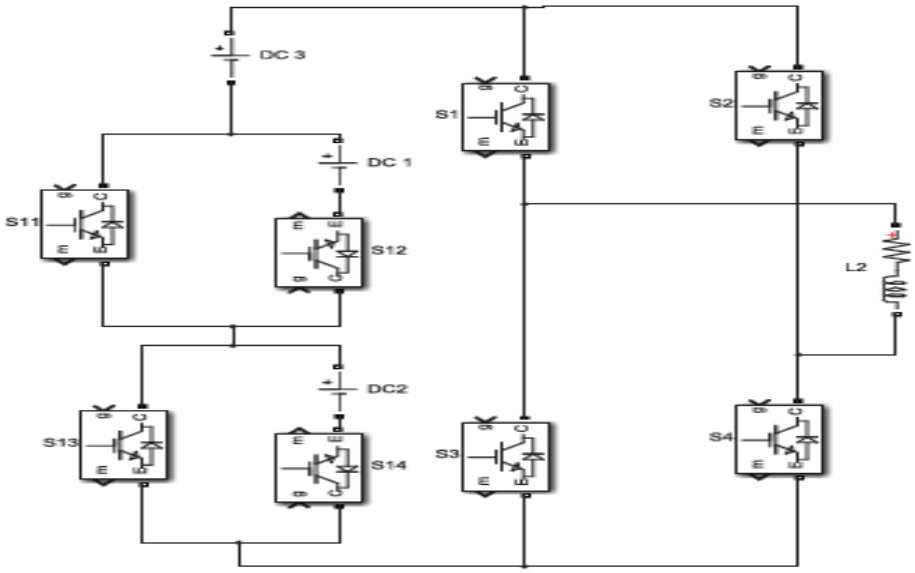

Fig.2.Multilevel scheme

symmetric with respect to neutral point, so the number of voltage levels is odd. Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency The cascaded H-bridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source Vdc. By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced. By closing the appropriate switches, each H-bridge inverter can produce three different voltages: +Vdc, 0 and -Vdc. It is also possible to modularize circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. The number of switches is reduced using the new topology. This circuit is simulated using the MATLAB software. The results are shown in the later sections in detail.

4. ANALYSIS

The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the voltage with fundamental frequency. Powering Mode: This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is Vdc, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is 2Vdc, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. When the output voltage is 3Vdc, the current pass comprises: upper supply, Q1, load, Q4, Q7, lower supply. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively. Free-Wheeling Mode Free-wheeling modes exist when one of the main switches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1. Regenerating Mode In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is

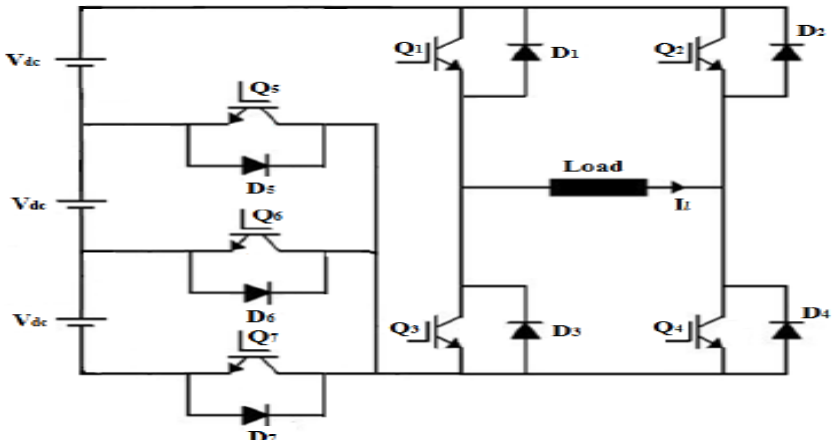

Fig.3.Proposed technology

negative during the positive half cycle and vice- versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4.

CONCLUSION

The proposed new cascaded H-bridge multilevel inverter fed induction motor using equal DC sources was developed and validated with the hardware. The fundamental switching scheme is employed using the microprocessor. By using the Selective harmonics elimination the firing angles are calculated and fed to the inverter for its operation. Finally using the power quality analyser the harmonics are measured and shown. In the conventional H- bridge multilevel inverter for seven level output 12 switches are needed whereas in new topology it is only 7.

REFERENCES

[1] Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad azem Bakhshizadeh, Naeem Farokhnia and S.Hamid Fathi, "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions on power electronics, vol. 27, no. 4, pp1689- 1696,2012.

[2] Damoun Ahmadi, KeZou, Cong Li, Yi Huang and Jin Wang, "A Universal Selective Harmonic Elimination Method for High-Power Inverters", IEEE Transactions on power electronics, vol. 26, no. 10,pp2743-2752,2011.

[3] FaeteFilho, Leon M. Tolbert, Yue Cao and BurakOzpineci, "Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation",IEEE Transactions on industry applications, vol. 47, no. 5, pp2117-2124,2011. [4] Hossein Sepahvand, Jingsheng Liao and Mehdi Ferdowsi, "Investigation on Capacitor Voltage Regulation in Cascaded H-Bridge Multilevel Converters With Fundamental Frequency Switching", IEEE Transactions on industrial electronics, vol. 58, no. 11,pp5102-5111,2011.

[5] Jason R. Wells, XinGengPatrick L. Chapman Philip T. Kreinand Brett M. Nee, "Modulation-Based Harmonic Elimination", IEEE Transactions on power electronics, vol. 22, no. 1,pp336-340, 2007.

[6] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler and M. A. Aguirre,"Selective Harmonic Mitigation Technique for Cascaded H-Bridge Converters with Non-Equal DC Link Voltages", IEEE Transactions on power electronics,pp1-9,2012.