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Structure Changed Cascaded H-Bridge Multilevel Inverter Topology with Reduced Switches

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Abstract

Multilevel Inverter widely used in high power industrial applications. This paper presents a new modified cascaded H-Bridge multilevel inverter with reduction of switching component. In traditional CHB inverters required more number of components, it seem to more complex control circuitry and bulky. Since Last few decade the researchers from all over world concentrating to improve the efficiency of Multilevel Inverter such as voltage balancing, reduction in components, modulation methods and control technique etc. The Proposed multilevel inverter output voltage level increasing by using less number of switches driven by the multicarrier modulation techniques. In this paper presents generalized structure, Operation, comparison with other traditional topology, Simulation results with MATLAB/SIMULINK and experimental results.

Index Terms*:* Cascaded H-Bridge (CHB) inverter, Multicarrier Modulation, Multilevel Inverter, Total Harmonics Distortion(THD).

1. INTRODUCTION

The different types cascaded multilevel inverter topology are available. A continuous development of multilevel converter to drive high voltage and high current industrial applications[1]. Nowadays, multilevel inverter are good solutions for power applications due to the fact that they can achieve high power using advanced power semiconductor[1]. However, the main disadvantage of the multilevel inverter more number of voltage level lead to increase the main switches, complexity of control technique and DC link capacitor voltage imbalance .There are several advantages compared with traditional or conventional power conversion methods. In multilevel inverter the isolated DC sources or bank of series capacitors are used. Isolated DC sources are available from the Photovoltaic cell or rectified. output from the three phase main supply. The Photovoltaic power conversion is one of the best suitable applications for cascaded H Bridge multilevel inverter. The smaller voltage level increase to lead the output quality in terms of reduce the voltage stress (dv/dt), Electromagnetic Interference (EMI) and draw input current with low distortion. However these advantages are very attractive to the industrial application and researchers all over the world contributing to improve the performance (control simplification, reduced THD, less number of components and ripple current) of multilevel inverter[1]. Since last decade the interest of the researchers are contributing to further development of a new multilevel converters topology with unique modulation strategies. The researchers from all over world introducing number of recent and advanced multilevel inverters topologies. There are several multilevel converters are commercialized for high power applications such as Flexible AC transmission systems(FACTS) Controllers, Train Traction,Automotive applications, renewable energy power conversion and transmission [2]-[4] etc. Some new multilevel inverter topologies are suggested with different operating methods with reduced switches[5]-[7]. Although the topology required different voltage rating switches compared with conventional CHB topology. It also required the target selection. Different approaches to reach simplified multilevel

converters are proposed and also number researchers are continuous to development of new multi level inverter topologies.Some other multilevel inverters, the [High-Level Multi step Inverter Optimization Using] advantage of requiring the same number of power transistors as the levels generated, and therefore, the semiconductors are reduced by half with respect to the previous topologies. though, it requires more number of switches compare with proposed multilevel inverter. There is also another topology by series / parallel switching the devices the number of voltage level increases which requires more number of switches than the proposed topology for the same levels. Some of the other topologies suffer from the additional components (diodes), complexities of capacitor balancing etc.,

In this paper mainly deal with new multilevel inverter topology is symmetrical topologies with minimum number of switches. There are asymmetrical topologies which require unequal voltage source. The major drawback of asymmetrical topology is various ratings of switches are required[8].

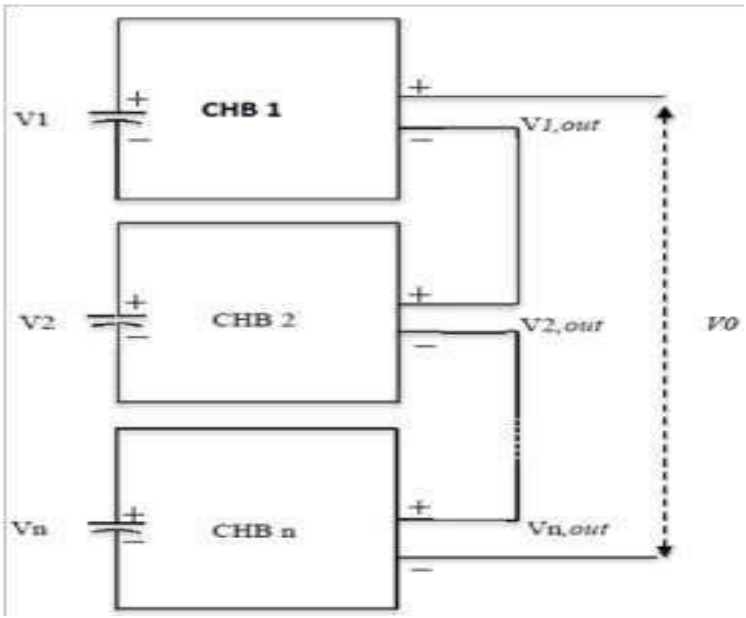


Figure1. General Structure of Cascaded H-Bridge Inverter

By using Multi-winding transformer can generate the multilevel output, more complex and cost of manufacturing the Multi winding transformer is high[9]-[12]. The topology includes with H-Bridge and Auxiliary bidirectional switch, to reduce the power circuit complexity and modulator circuit development[8], Even though the number of switches are more compare with the proposed topology.

2. PROPOSED MULTILEVEL INVERTER TOPOLOGY:

A. General Description:

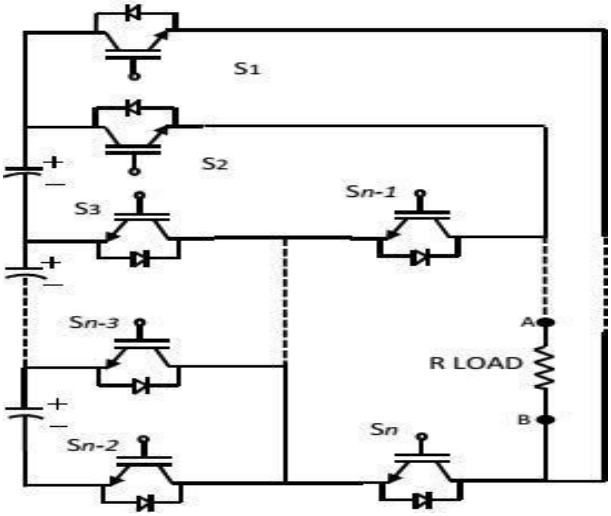
This topology is a simplified CHB inverter symmetric topology. The main advantage of proposed topology is less number of switches comp ared with conventional multilevel inverter.

Number of Level (m)= 2n+1.....(1)

Number of Main Switches (n switch) = ((m-1)/2) + 4.....(2)

Where 'm' is the number of output voltage level, 'n' number DC source switches. Figure.1 shows the general circuit diagram of proposed multilevel inverter. If number levels increases add one switch for each level, simple control circuitry. The Unique modulation strategies are applicable for this topology. The numbers of switches are required for each level and switches can be calculated from the above equations (1) and (2). To get a Positive half, properly turn ON the switches and the current flow from the point A to B will generate a positive polarity, the flow from B to A will generate the negative polarity as shown in Figure 2(a). In general, in order to achieve an equal voltage steps, the equal and same dc source voltage to be use. The unequal Vdc generate the different voltage steps.

There are several multilevel inverters are commercialized for high power applications such as Flexible AC Transmission Systems (FACTS) Controllers, Train Traction, Automotive applications, renewable energy power conversion and transmission etc.



S1	S2	S3	S4	S5	S6	S7	Voltage Level
1	0	1	0	0	0	1	+Vdc
1	0	0	1	0	0	1	+2Vdc
1	0	0	0	1	0	1	+3Vdc
0	0	0	0	0	0	0	0
0	1	1	0	0	1	0	-Vdc
0	1	0	1	0	1	0	-2Vdc
0	1	0	0	1	1	0	-3Vdc

3. MODULATION TECHNIQUE:

The proposed system can be run with existing modulation technique Alternative Phase Opposition Disposition (APOD). If M=7 (M is number of Level) the required carrier waveforms is M-1=6

B. Circuit Description:

The following output voltage levels required to generate seven level voltage *+Vdc, +2Vdc, +3Vdc, 0,-Vdc,-2Vdc,-3Vdc.*

(i) Positive Polarity:

For Vdc the S2, S7, S3 switches are ON. The S1 is connected in positive terminal of the load and S3 is connected with negative terminal of the load through S7.for +2Vdc and+3Vdc,switches S2 and S7 are continuously ON for positive half cycle the switches S4 and S5 are Turn ON according to the

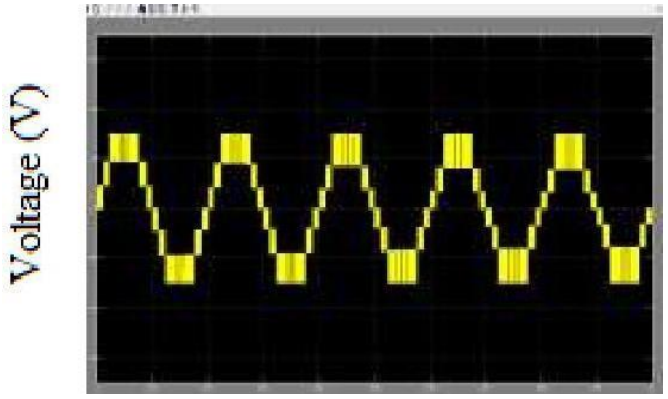
(ii) Negative Polarity:

For -Vdc the S1, S6, S3 switches are ON. The S2 is connected in positive terminal of the load and S3 is connected with negative terminal of the load through S6.Such a way that switches S1 and S6 are continuously ON for positive half cycle the switches, S4 and S5 are Turn ON according to the PWM signals as shown in Table1. There are several unique carrier based PWM (CBPWM) techniques are available for multilevel inverter. One of the most

common methods is APOD (Alternative Phase Opposition Disposition).APOD carriers in adjacent side are phase shifted by180º and CBPWM required *S-1* triangular carrier waveform and S is the number of voltage level as shown in Figure 2(d)

4. SIMULATION RESULTS:

The simulated 7 level output waveform in figure3.as.,



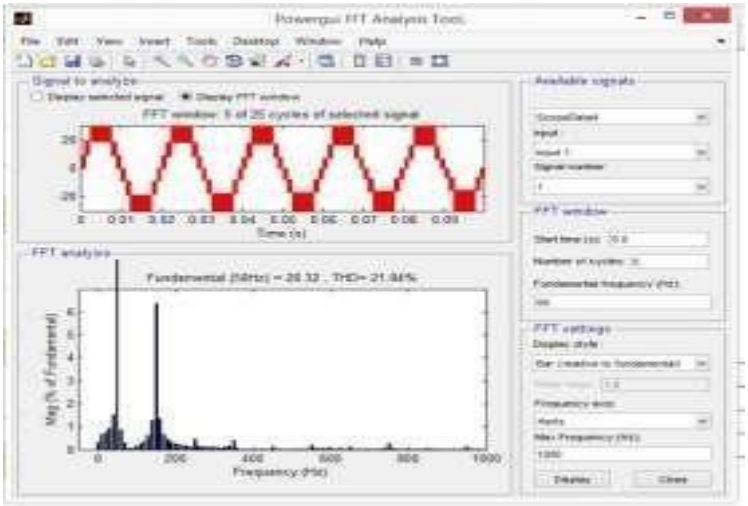
(i) Fast Fourier Transform(FFT) :

FFT is an algorithm to compute the discrete fourier transform (DFT) and Inverse discrete fourier transform(IDFT). A fourier transform converts time to frequency and vice-versa.FFT rapidly such transformations by
factorizing the DFT matrx into a product of sparse (mostly zero) factors.

(ii)Analysis For Total Harmonic

Distorion(THD) :

In the Matlab,an option for performing Fast Fourier Transform (FFT) analysis to quantify the THD in the model. By giving, the real values as input to these hardware elements in the model,the real time harmonic distorton is obtained. By doing so, the THD for the proposed model is 21.84 % The THD Analysis by matlab is shown in figure4 as.,



CONCLUSION

This paper analyzed new multilevel inverter topology with reduced number of switches shown in figure 2(a) and 2(b). The outputs are verified by hardware setup as shown in figure.

- The Conduction losses will be less, if number of Switches is reduced.
- The size of the multilevel inverter will be compact than other inverters.
- The overall cost will be reduced by reducing the number of main switches.
- The application can be AC drive, Photovoltaic and FACTS devices etc.,

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